WHAT IS CLAIMED IS:

1. A method of operating a transistor device comprising:

floating a gate electrode of the transistor device;

applying a voltage between a drain and a source electrode of the transistor device to cause a burned region in a channel region of the transistor device, even after the voltage is removed.

2. The method of claim 1 wherein the burned region provides a low impedance path between the drain and source electrodes.

3. The method of claim 1 wherein the burned region extends from the drain to the source and has a deeper depth closer to the drain than the source electrode.

4. The method of claim 1 wherein an impedance for the transistor device is about five times or greater than that for transistor device with the burned region.

5. A semiconductor device comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a polysilicon gate formed on the substrate and positioned between the drain and source regions;

a burned region, formed after a burning operation, formed beneath the polysilicon in the substrate between the drain and source, wherein the burned region provides a low-impedance path between the drain and source, even when the polysilicon gate is floating.

6. The semiconductor device of claim 5 wherein an impedance for the semiconductor device from drain to source is about five times or greater than that for the semiconductor device without the burned region.

7. The semiconductor device of claim 5 wherein the low-impedance path provides an impedance of about 660 ohms or less.

8. The semiconductor device of claim 5 wherein a channel length of the semiconductor device is about the same as a length of the burned region, and a depth of the burned region is deeper closer to the drain than closer to the source.

9. The semiconductor device of claim 5 wherein the burned region comprises more defects and dislocations than before forming the burned region.

10. A read-only memory integrated circuit comprising memory cells formed using the semiconductor device recited in claim 5.

11. An electronic system comprising semiconductor devices as recited in claim 5.

12. A method of operating an electronic system comprising programming one or more transistor devices according to the method recited in claim 1.

13. An integrated circuit comprising:

a plurality of row lines and column lines arranged in rows and columns;

an array of memory cells, each memory cell comprising a drain electrode coupled to one of the plurality of column lines and a source electrode coupled to one of the plurality of row lines, wherein a memory cell has a first state where the memory cell has a burned region in its channel to provide a lower impedance path than when the memory cell is in a second state; and

a decoder circuit, coupled to the plurality of row lines, to select a row in the array of memory cells.

14. An integrated circuit comprising:

a first interconnect line;

a second interconnect line;

a programmable switch comprising a transistor coupled between the first and second interconnect lines, wherein the programmable switch has a first state and a second state, and in the second state, the transistor has a burned region in its channel region, providing a lower

impedance path between the first interconnect line and the second interconnect line in the second state than in the first state.

15. The integrated circuit of claim 13 wherein the memory cells are at least one of MOSFET transistors, n-type MOSFET transistors, or p-type MOSFET transistors.

16. The integrated circuit of claim 14 wherein the second state, the memory cell has an impedance of about 660 ohms or less.

17. The integrated circuit of claim 14 wherein in the first state, the memory cell has an impedance of about 3 mega ohms or greater.

18. The method of claim 1 wherein the transistor device has a width of 0.22 microns or less and a length of 0.13 microns or less.

19. The method of claim 1 wherein the transistor device is at least one of a MOSFET transistor, n-type MOSFET transistor, or p-type MOSFET transistor.

20. The method of claim 1 wherein the applying a voltage comprises:

applying a breakdown voltage to the drain electrode of the transistor device; and

after applying the breakdown voltage, applying a burning voltage to the drain electrode of the transistor device, wherein the burning voltage is greater than the breakdown voltage.

21. A circuit comprising:

an operational amplifier circuit having inputs and an output;

a transistor, coupled between an input and the output, having a programmable resistance and a first state and a second state, wherein in the second state, the transistor has a burned region in its channel region, providing a lower impedance path between the input and the output in the first state.

22. A circuit comprising:

a first line and a second line;

a transistor, coupled between the first and second lines, having a programmable resistance and a first state and a second state, wherein in the second state, the transistor has a

burned region in its channel region, providing a lower impedance path between the input and the output in the first state.